

Vivek Shah

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OBJECTIVE: To obtain a full-time position in field of Hardware Engineering/ Analog and Digital system Design, ASIC design, Verification and Validation, Embedded System Design where I can enhance my knowledge and pioneer an innovative technological development.

EDUCATION: Master of Science in Electrical Engineering Graduation Date: May 2016
Southern Methodist University, Dallas, TX GPA: 3.26/4

Bachelors in Instrumentation and Control Engineering Graduation Date: May 2013
Gujarat Technological University, Gandhinagar, Gujarat, India CGPA: 7.17/10

RELEVANT COURSES: Embedded Wireless Design ,Digital System Design ,VLSI Design and Advance VLSI Design ,Microcontroller Architecture & Interfacing ,Semiconductor Device & Circuit , Foundation of formal verification and validation ,Transistor Integrated Circuits ,VLSI Algorithms

TECHNICAL SKILLS: **Computer Languages:** C, C++, Verilog, VHDL, Python, ARM & x86 Assembly, System Verilog, JAVA

Technologies: RTOS,ADC, I2C, USB, UART, AMBA, CAN

Software: Altium, Xilinx Studio, Quartus, Cadence Design Studio, Keil, Proteus, MPLab, Matlab

ENGINEERING PROJECTS:

8 bit Multiplier Transistor Level design and it's Layout:

- Designed multiplier which would work on low power. Carry Save addition methodology is used for 8 bit multiplication. Design worked on as low as 1.2V with power dissipation of 192.2μW and delay was 2.05ns.

Distributed Beamforming Feasibility Testing:

- Demonstrated the effectiveness of distributed beamforming vs conventional way of transmission in different scenarios.
- Our paper provided overview of related work focused on implementing distributed beamforming. Our test scenarios and its result to test effectiveness of distributed beamforming vs conventional way of transmission.

Matrix Multiplier:

- Designed digital system to multiply a 3x4 matrix with its transpose. Designed two main block for this circuit: Controller and Data path. The circuit computed $B = A^T * A$ (3x4 matrix).
- Design were done in Verilog and software used was Altera Quartus.

2.4 GHz CMOS Receiver:

- Designed 2.4GHz CMOS receiver. CMOS receiver contains four major block, an LNA, Mixer, VCO and low pass filter. Designed 2.4GHz Single ended and Differential LNA with gain of 21.5dB and noise figure of 847.12mdB, 1.2GHz Local oscillators, and Mixer based on Gilbert cell double balanced topology.

For More Projects and Details about Project please visit: www.vivekkshah.com/projects/

TECHNICAL EXPERIENCE:

PION (Parth) Electronics, Ahmedabad, Gujarat, India

08/12 - 06/14

- Providing Technical support
- Managing and optimizing manufacturing process
- Successfully developed and deployed embedded system for Servo Voltage Stabilizer:
- Worked as a development engineer and Primary responsibility was to create and test voltage and current sensing circuits and to develop software in C/C++ for controller PIC16f877A, LCD display and keypad. Developed schematic and PCB for control card and power card.

ACTIVITIES:

- Organized two sports competition in my dorm which had six different games with more than 60 participant.
- Successfully managed library of my dorm for two years and expanded it from carrying 100 books to more than 300 books for different engineering, medical, management, business and finance field to help the students of our dorm.